REMARKS

The 35 U.S.C. §102(e) Rejections

The Examiner rejected claims 1-49 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,111,245 to Wu et al. (Wu).

The test for anticipation is symmetrical to the test for infringement and has been stated as: "That which would literally infringe [a claim] if later in time anticipates if earlier than the date of invention." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989); *Connell v. Sears Roebuck & Co.*, 722 F.2d 1542, 1548, 220 U.S.P.Q. 1931, 1938 (Fed. Cir. 1983). Moreover, the single source must disclose all of the claimed elements "arranged as in the claim." *Structural Rubber Prods. Co. v. Park Rubber Co.*, 749 F.2d 707, 716, 223 U.S.P.Q. 1264, 1271 (Fed. Cir. 1984). Also, each and every element as set forth in the claim must be found, either expressly or inherently described, in a single prior art reference. MPEP 2131.

Independent claims 1, 12, 22, and 31 have been amended to recite, in part, a plurality of storage pixel sensors disposed on a semiconductor substrate, each of the plurality of storage pixel sensors comprising . . . a capacitive storage node, coupled to said source of said source-follower transistor, comprising the input of a readout amplifier transistor having an output. No new matter has been added to the application. Support for the amendment may be found on page 8, lines 15 through page 11, line 14, describing pixel sensor 10, capacitive storage node 26 and source follower transistor 30, and Figure 1.

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Wu, in Figure 2, illustrates an image sensor with a pixel array, a row decoder, pixel sensors (presumably number 24), sensing amplifier 22, and a column decoder. Col. 2, lines 10-15. The active pixel circuit of Wu is illustrated in Figure 3. Col. 2, lines 18-19. Diode D2 in Figure 3 is coupled to common address BL. The sensing amplifiers (shown in Figure 5), which are clearly separate and distinct from the pixel sensors in Figure 3, are coupled to each common address BL (also see Figure 2). Therefore, Wu fails to anticipate a plurality of storage pixel sensors disposed on a semiconductor substrate, each of the plurality of storage pixel sensors comprising . . . a capacitive storage node, coupled to said source of said source-follower transistor, comprising the input of a readout amplifier transistor having an output, as recited in independent claims 1, 12, 22, and 31.

Claims 1, 12, 22, and 31 are independent claims and are in condition for allowance. Claims 2-11, 13-21, 23-30, and 32-38 depend from the above claims and are in condition for allowance as well.

Claim 39 recites, in part, a pixel sensor disposed on a semiconductor substrate comprising . . . an exposure transistor having a source coupled to said output of said source-follower transistor and drain coupled to a global current-summing node, said exposure transistor having a control gate coupled to a saturation level control voltage. In rejecting claim 39, the Examiner referenced claims 1 and 11. With respect to claim 11, the Examiner maintains that Wu discloses an exposure transistor (M4 in Figure 3) having a source coupled to said output of said source-follower transistor (M3) and drain coupled

to a global current-summing node (VDD in Figure 3), said exposure transistor having a control gate coupled to a saturation level (WL signal) control voltage.

Applicant respectfully disagrees with the Examiner's position. The output of a source-follower transistor is the source, not the drain, hence the term "source-follower." The source of transistor M4 of Wu is connected to the drain of transistor M3. In order to disclose an exposure transistor having a source coupled to said output of said source-follower transistor, as recited in claim 39, the source of transistor M4 would have to be connected to the source of transistor M3. This is not the case.

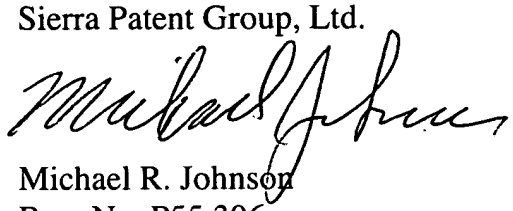
In support of Applicant's assertion, a description for a source-follower configuration is included from Microelectronic Circuits, Third Edition, by Sedra/Smith. The output (source) voltage of a transistor in a source-follower configuration follows the input (gate) voltage. The Examiner will notice that output voltage (v_o), is measured from source to ground, and is a function, in this example, of the gate voltage (v_i), source-gate resistance ($1/g_m$), and source-body resistance ($1/g_{mb}$). Applicant maintains that the output of a source-follower transistor cannot be reasonably interpreted to mean its drain terminal. If the Examiner maintains the rejection then Applicant respectfully requests that the Examiner explain the reasoning more thoroughly. Wu fails to disclose claim 39.

Claims 40-49 depend from claim 39 and are patentable in light of Wu.

Applicant respectfully requests that the Examiner allow all the claims and direct the application to issue.

In view of the foregoing, consideration and an early allowance of this application are earnestly solicited.

Respectfully submitted,
Sierra Patent Group, Ltd.



Dated: February 9, 2004

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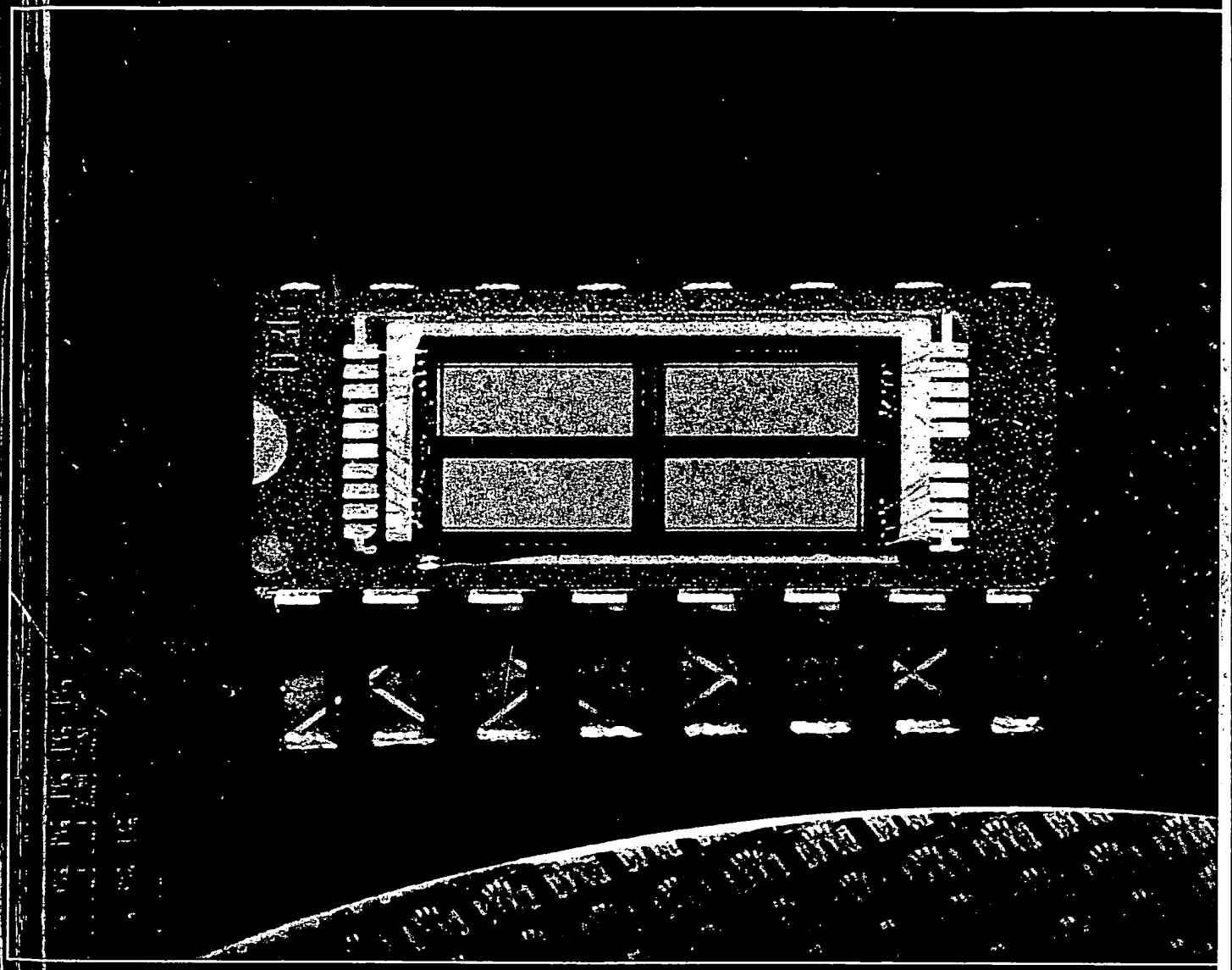

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ABOUT THE COVER

In the background is a processed wafer of silicon on which a large number of identical circuit chips are fabricated. When cut from such a wafer, a chip can be housed in a package such as the one shown here with its cover removed. This single chip is a segmented memory array with a very large number of active devices in a variety of intricate circuit structures. The growing need for efficient and reliable low-cost components such as these underlies the importance of the various circuit design and circuit analysis techniques discussed in this text.

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Library of Congress Cataloging-in-Publication Data

Sedra, Adel S.
Microelectronic circuits/Adel S. Sedra, Kenneth C. Smith.—3rd ed.
p. cm.—(The Holt, Rinehart, and Winston series in electrical engineering)
Includes bibliographical references and index.
ISBN 0-03-051648-X
1. Electronic circuits. 2. Integrated circuits. I. Smith, Kenneth Carless. II. Title. III. Series: HRW series in electrical engineering.
TK7867.S39 1990
621.381'5—dc20 90-24195
CIP

Cover Credit: Computer Chip/The Stock Market © 1989 Ted Horowitz

Printed in the United States of America

Microelectronic Circuits, 3 ed.

0-03-051648-X

Library of Congress Catalog Card Number: 0-03-051648-X 90-24195

3 0 1 6 9 8 7 6 5 4

Prereq

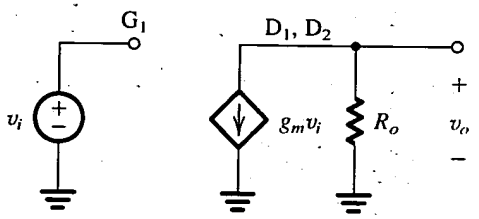
Organi

Exercises 5.38 For the CMOS amplifier of Example 5.14, find the small-signal voltage gain for $I_{REF} = 25\ \mu A$ and $400\ \mu A$.

Ans. -200 V/V; -50 V/V

5.39 For small-signal operation, the CMOS amplifier of Fig. 5.59(a) can be represented as a transconductance amplifier (Section 1.5). Sketch the amplifier equivalent circuit.

Ans. See Fig. E5.39



$$g_m = g_{m1} = \sqrt{2(\mu_n C_{OX})(W/L)_1 I_{REF}}$$
$$R_o = r_{o1} \parallel r_{o2}$$

Fig. E5.39

The Source Follower

The source-follower configuration was studied in Section 5.8. In the design of MOS IC amplifiers, the source follower is used as a buffer to obtain a low output resistance. Figure 5.60(a) shows a source follower as it is commonly connected in an IC amplifier. To calculate the small-signal voltage gain and output resistance, we show in Fig. 5.60(b) the circuit with the dc voltage sources replaced with grounds and the dc current source replaced with an open circuit. Also shown are the resistance $1/g_m$, which is the equivalent resistance seen between source and gate, looking into the source; the resistance $1/g_{mb}$,

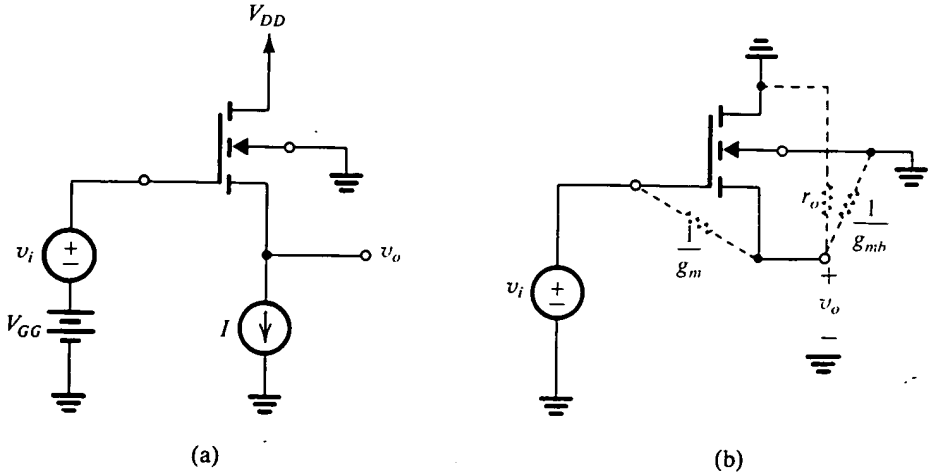


Fig. 5.60 (a) Source-follower circuit. (b) Source follower with the source-to-gate equivalent resistance (looking into the source), the source-to-body equivalent resistance (looking into the source), and the drain-to-source resistance shown.

Exercise
$V_t = 1$ V
Ans. 0.9

5.10 FE

which is the equivalent resistance between source and body, looking into the source; and the source-to-drain resistance r_o. Extreme caution should be exercised in using this equivalent circuit: $1/g_m$ in the resistance looking into the source; the resistance looking into the gate is infinite, since the gate current is zero. Thus the input resistance of the source follower is infinite.

The output voltage v_o appears across the total resistance between source and ground. This is the parallel equivalent of r_o and $1/g_{mb}$. To find the voltage gain we use the voltage-divider rule

$$\frac{v_o}{v_i} = \frac{[(1/g_{mb})//r_o]}{(1/g_m) + [(1/g_{mb})//r_o]} \tag{5.103}$$

If $r_o \gg 1/g_{mb}$, we obtain

$$\frac{v_o}{v_i} \simeq \frac{g_m}{g_m + g_{mb}} \tag{5.104}$$

Substituting $g_{mb} = \chi g_m$ gives

$$\frac{v_o}{v_i} = \frac{1}{1 + \chi} \tag{5.105}$$

Thus the body effect reduces the gain from approximately unity to the value given by Eq. (5.105). Note that this gain value is obtained with no load; it is the open-circuit voltage gain. It can be used together with the output resistance R_o of the source follower, to obtain the gain when a load is connected. The output resistance is the resistance between the source and ground with v_i reduced to zero. Short-circuiting the signal source v_i in Fig. 5.60(b), we see that

$$R_o = (1/g_m)//(1/g_{mb})//r_o \tag{5.106}$$

Exercise 5.40 For the source-follower circuit of Fig. 5.60(a), let $W = 100\ \mu$m, $L = 8\ \mu$m, $\mu_n C_{OX} = 100\ \mu$A/V^2, $V_t = 1$ V, $V_A = 100$ V, $I = 0.5$ mA, and $\chi = 0.1$. Calculate the open-circuit voltage gain and the output resistance.

Ans. 0.91 V/V; 810 Ω

5.10 FET SWITCHES

Field-effect transistors can be used as switches for both analog and digital signals. To understand the basis for the operation of the FET as a switch, consider the circuit in Fig. 5.61(a). Here an NMOS transistor is to be operated as a switch between node X and ground. That is, when the switch is open, node X is disconnected from ground, and when the switch is closed node X is connected to ground. The NMOS switch is controlled by its gate voltage v_G, which takes one of two levels: $V_1 < V_t$ and $V_2 > V_t$. Figure 5.61(b) shows a graphical construction to determine the operating point corresponding to each of the two levels of the control signal.

When $v_G = V_1$, the transistor will be cut off and the operating point will be that

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